FIG. 1A

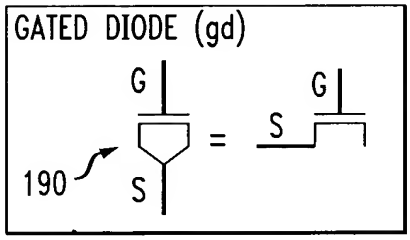


FIG. 1B

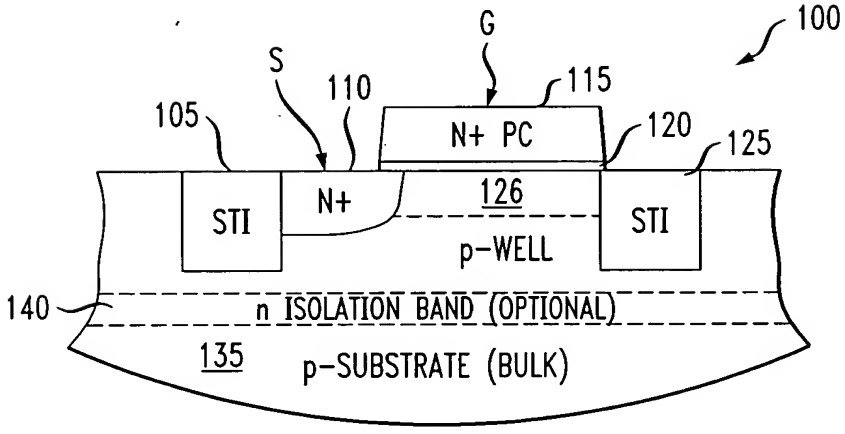


FIG. 2A

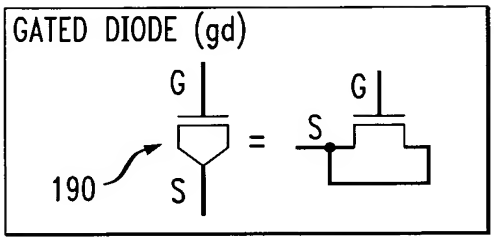

GATED DIODE (gd)
G
S
190
=
G
S

FIG. 2B

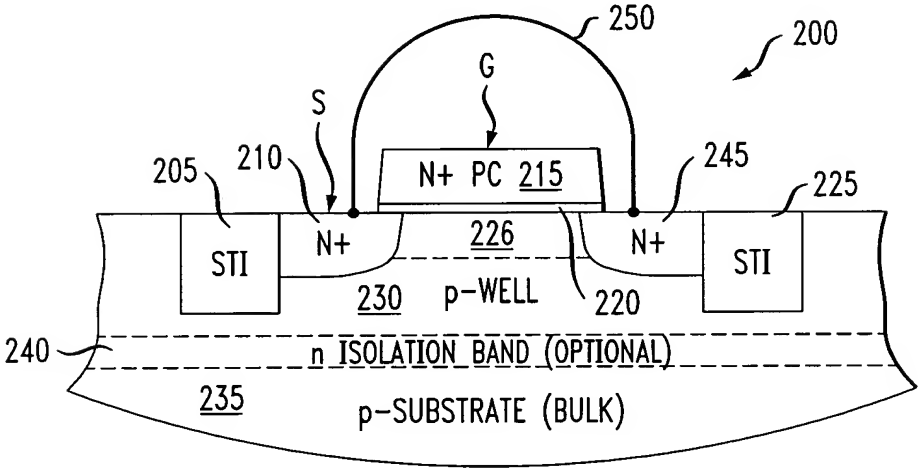

250
200
G
S
205
210
N+ PC 215
245
225
STI
N+
226
N+
STI
230
p-WELL
220
240
n ISOLATION BAND (OPTIONAL)
235
p-SUBSTRATE (BULK)

FIG. 3A

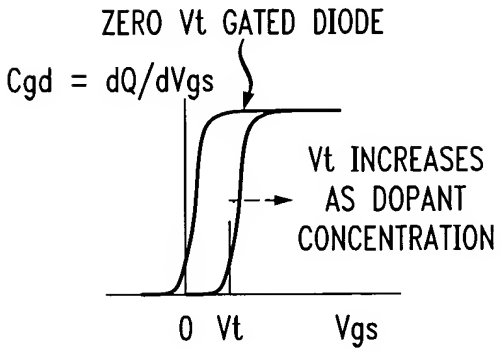


FIG. 3B

GATED DIODE CAPACITANCE vs GATE-TO-SOURCE VOLTAGE (Vgs)
EACH CURVE REPRESENTS A DIFFERENT GATED DIODE GATE SIZE.
THRESHOLD VOLTAGE = 0.2 V

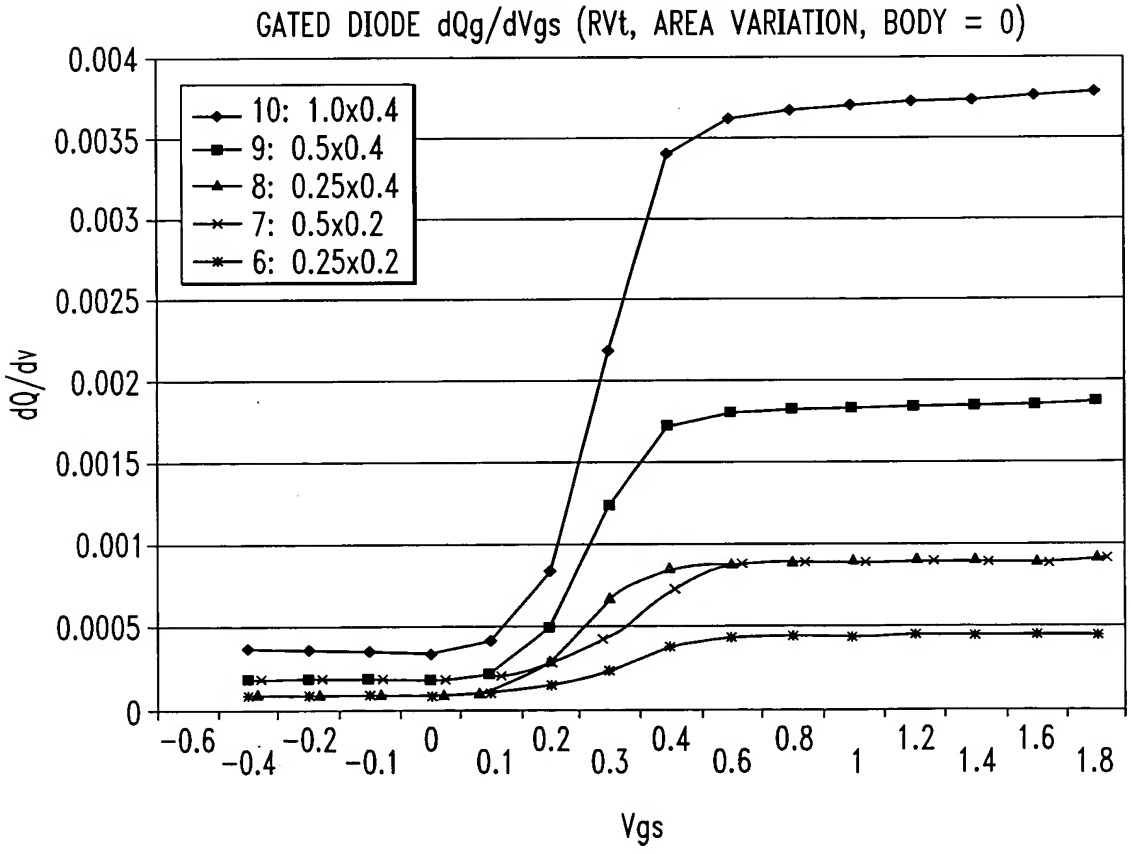


FIG. 4A

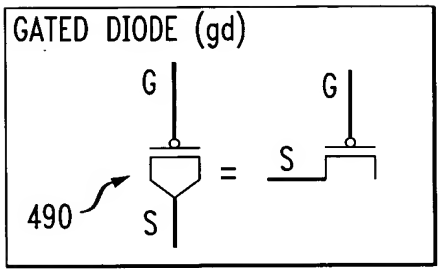

GATED DIODE (gd)
G
G
S
=
490
S

FIG. 4B

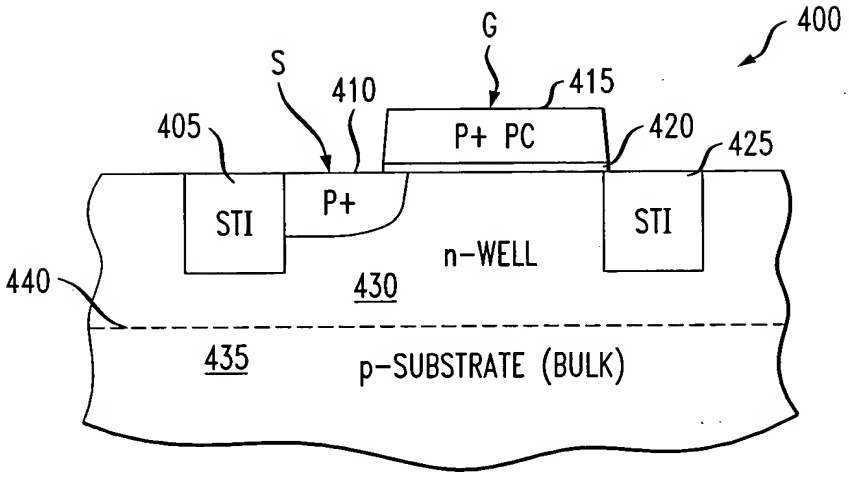

400
G
S
410
415
405
P+ PC
420
425
STI
P+
STI
n-WELL
440
430
435
p-SUBSTRATE (BULK)

FIG. 5A

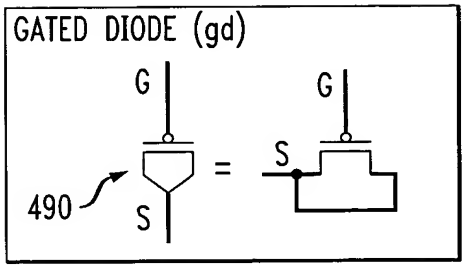

GATED DIODE (gd)
G
S
490
=
G
S

FIG. 5B

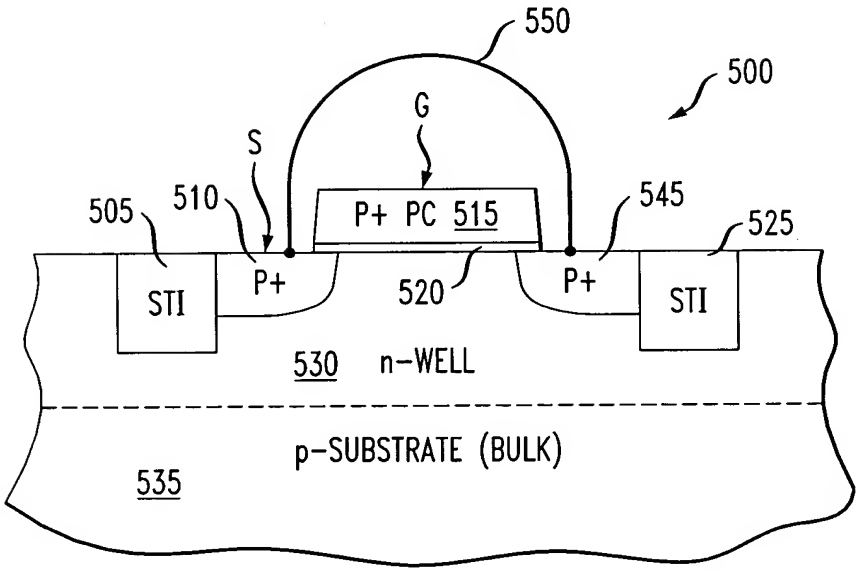

550
500
G
S
505
510
P+ PC 515
545
525
STI
P+
520
P+
STI
530 n-WELL
p-SUBSTRATE (BULK)
535

FIG. 6

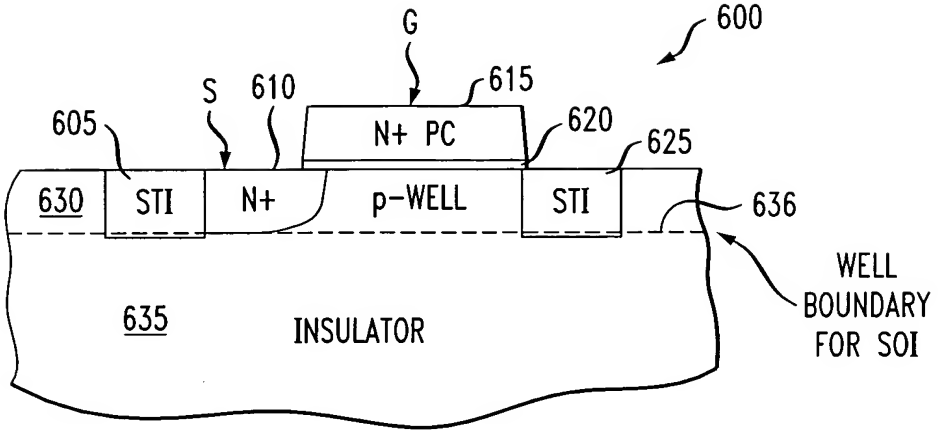

G
600
S
610
615
605
N+ PC
620
625
630
STI
N+
p-WELL
STI
636
WELL
BOUNDARY
FOR SOI
635
INSULATOR

FIG. 7

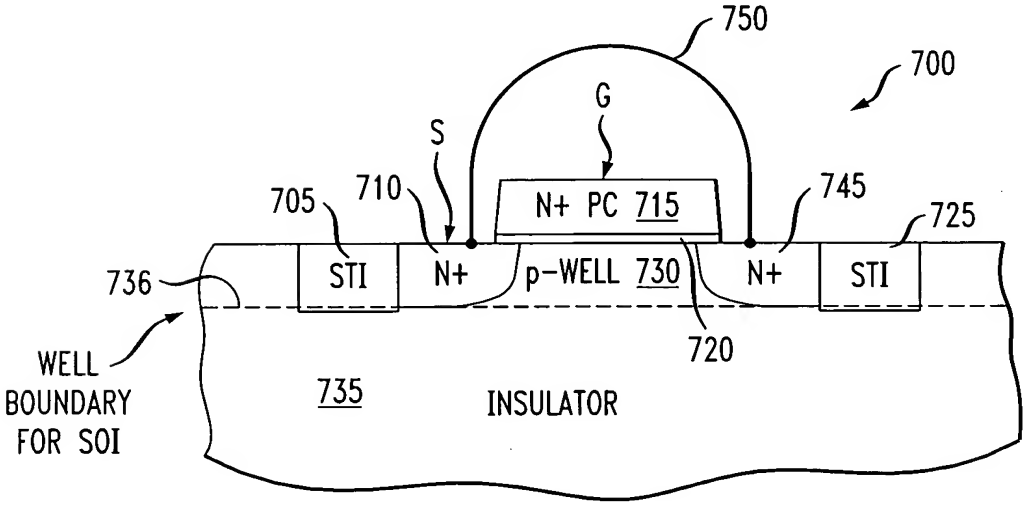

750
700
G
S
705
710
N+ PC 715
745
725
736
STI
N+
p-WELL 730
N+
STI
720
WELL
BOUNDARY
FOR SOI
735
INSULATOR

FIG. 8

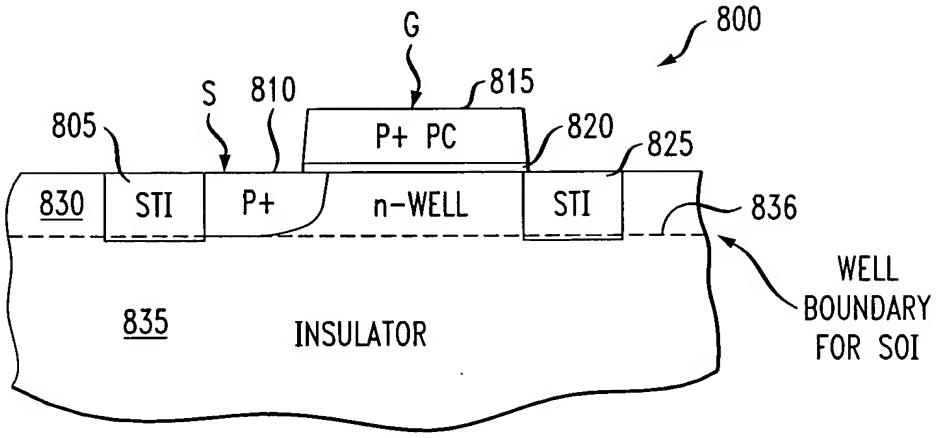


FIG. 9

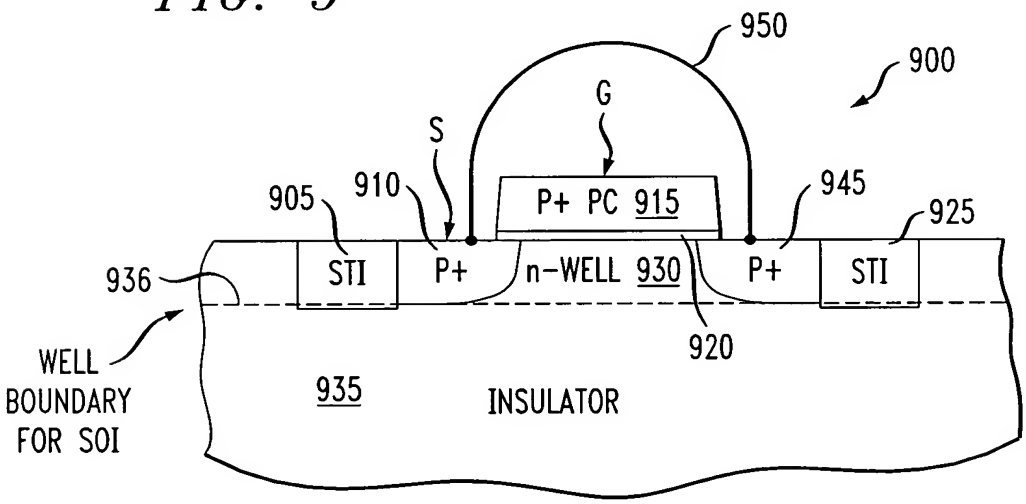


FIG. 10

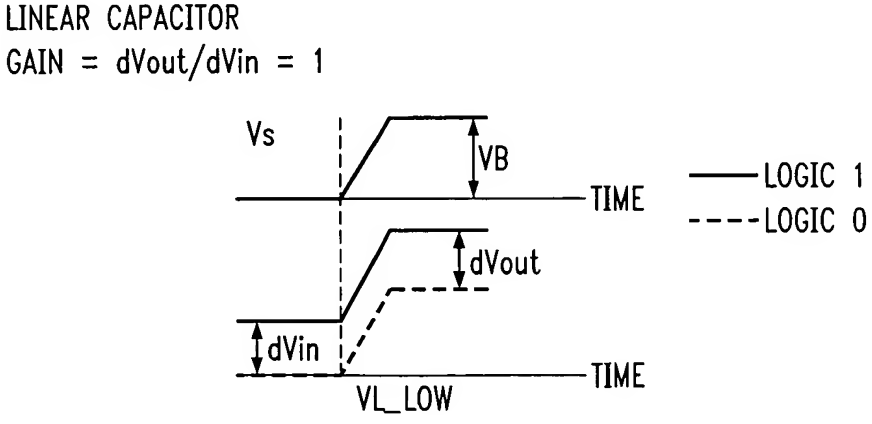


FIG. 11A

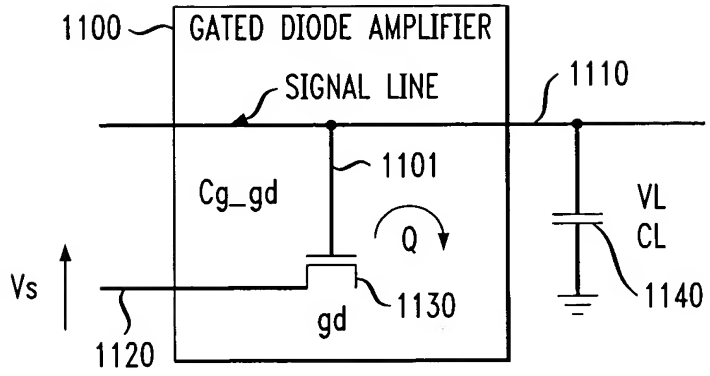


FIG. 11B

GATED DIODE AMPLIFIER REPRESENTATIVE CIRCUIT

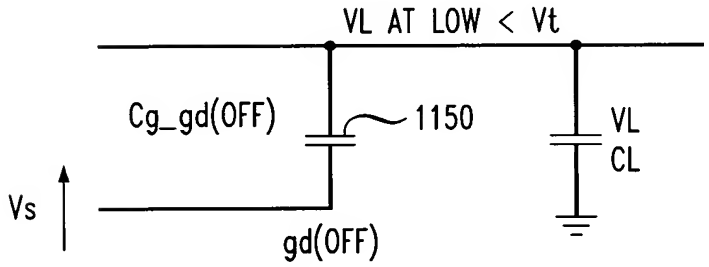


FIG. 11C

GATED DIODE AMPLIFIER REPRESENTATIVE CIRCUIT

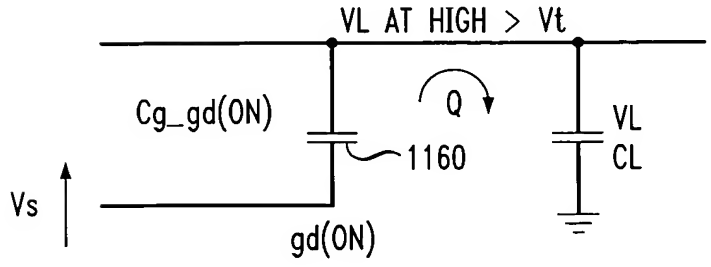


FIG. 12A

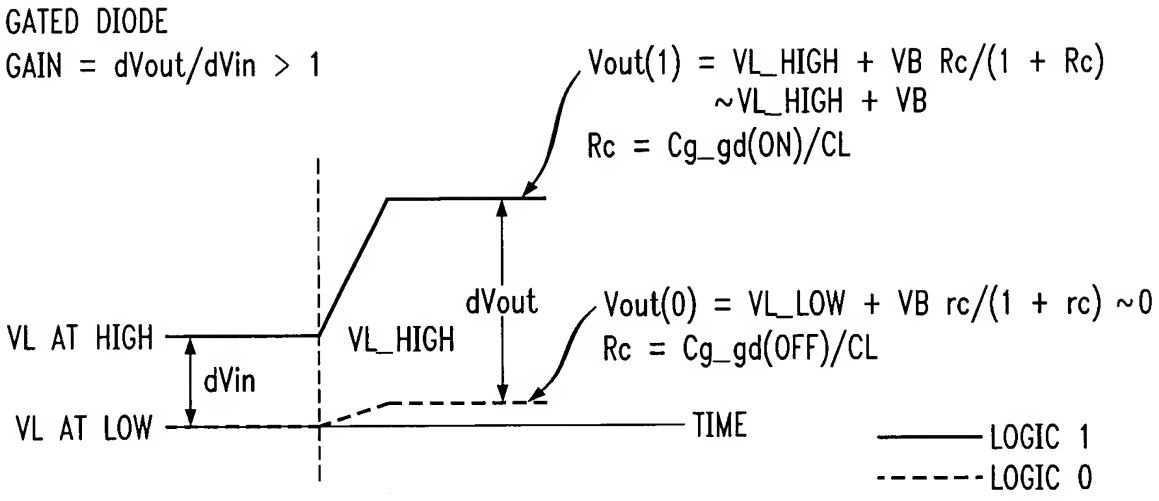


FIG. 12B

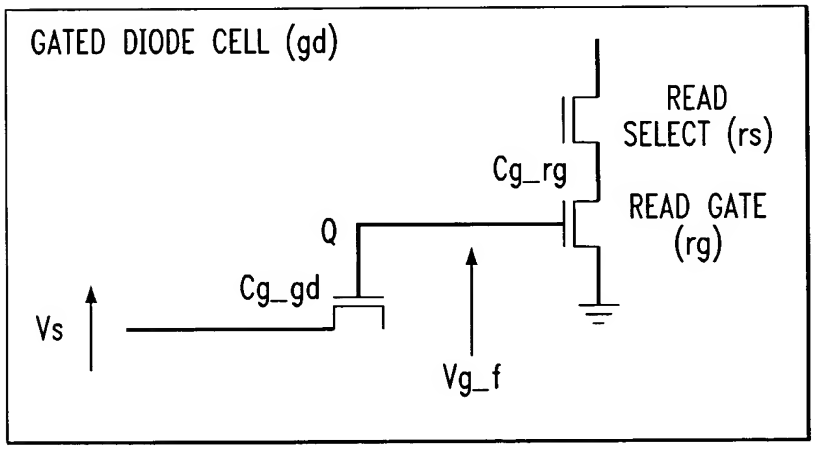


FIG. 12C

$Rc = Cg\_gd/Cg\_rg$
$GAIN = Vg\_f/Vg\_i$

$GAIN = 1 + Rc - (Vt\_gd/Vg\_i)\ Rc \sim 1 + Rc$ COMPLETE CHARGE TRANSFER (FOR SMALL Rc)
$GAIN = (1 + Vs/Vg\_i)\ Rc/(1 + Rc)$ CONSTRAINED CHARGE TRANSFER (LARGE Rc)

$Vg\_i = 0.4\ V,\ Vt\_gd = 0$

EXEMPLARY OPERATING POINT

Cg_gd/Cg_rg	0.01	0.1	1	2	5	10	100	
$1 + Rc$	1.01	1.1	2	3	6	11	101	
$Rc/(1 + Rc)$	0.01	0.09	0.5	0.67	0.83	0.91	0.99	
$(1+Vs/Vg\_i)Rc/(1+Rc)$	0.035	0.32	1.75	2.35	2.91	3.19	3.47	$Vs/Vg = 2.5$
$(1+Vs/Vg\_i)Rc/(1+Rc)$	0.04	0.36	2.00	2.68	3.32	3.64	3.96	$Vs/Vg = 3$
GAIN	1.01	1.1	2	2.68	3.32	3.64	3.96	$Vs/Vg = 3$
CHARGE TRANSFER	←--- COMPLETE ---→			←----- CONSTRAINED ----→				

FIG. 12D

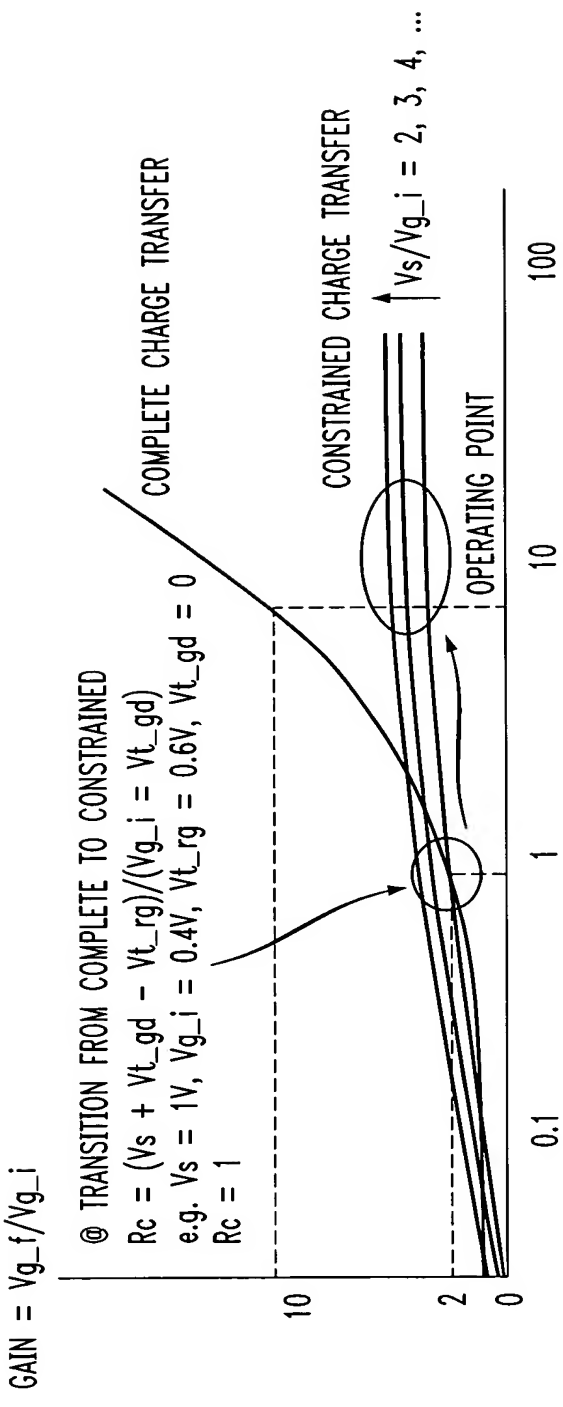

GAIN = Vg_f/Vg_i
@ TRANSITION FROM COMPLETE TO CONSTRAINED
Rc = (Vs + Vt_gd - Vt_rg)/(Vg_i = Vt_gd)
e.g. Vs = 1V, Vg_i = 0.4V, Vt_rg = 0.6V, Vt_gd = 0
Rc = 1
COMPLETE CHARGE TRANSFER
CONSTRAINED CHARGE TRANSFER
Vs/Vg_i = 2, 3, 4, ...
OPERATING POINT
10
2
0
0.1
1
10
100
Rc = Cg_gd/Cg_rd

FIG. 13

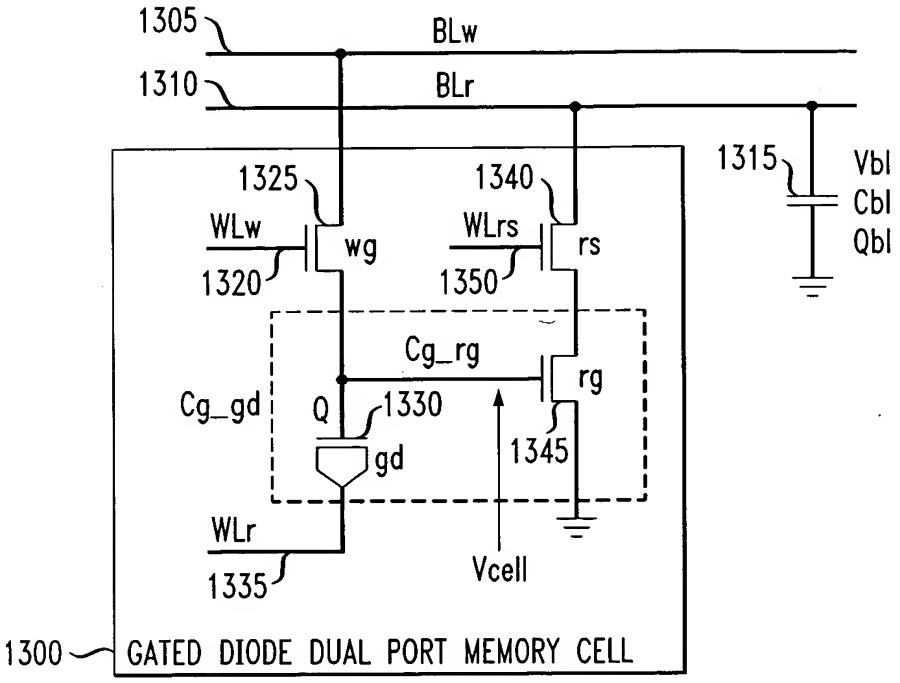

1305
BLw
1310
BLr
1315
Vbl
Cbl
Qbl
1325
1340
WLw
wg
WLrs
rs
1320
1350
Cg_rg
rg
Cg_gd
Q
1330
gd
1345
WLr
1335
Vcell
1300
GATED DIODE DUAL PORT MEMORY CELL

FIG. 14

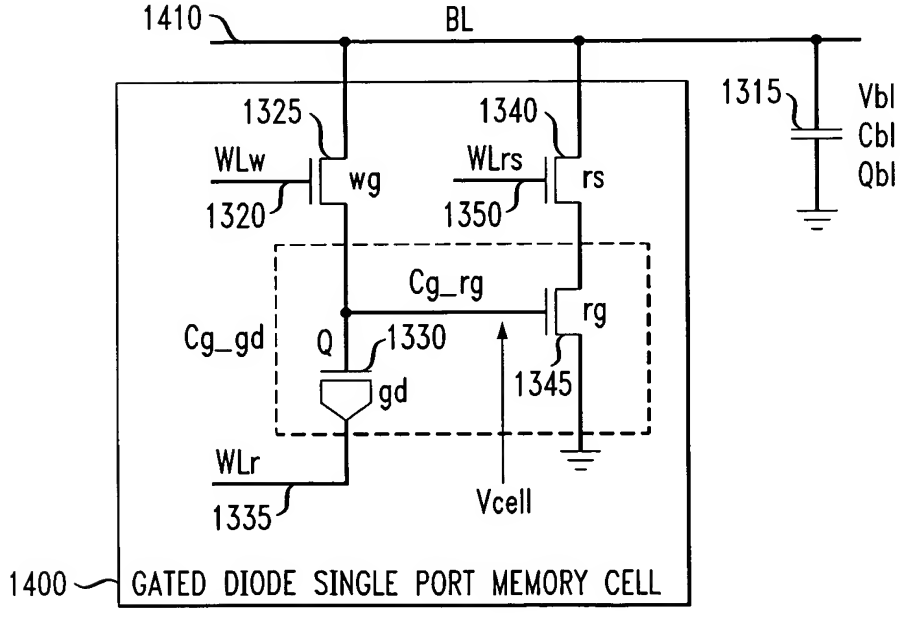

1410
BL
1315
Vbl
Cbl
Qbl
1325
1340
WLw
wg
WLrs
rs
1320
1350
Cg_rg
rg
Cg_gd
Q
1330
gd
1345
WLr
1335
Vcell
1400
GATED DIODE SINGLE PORT MEMORY CELL

FIG. 15

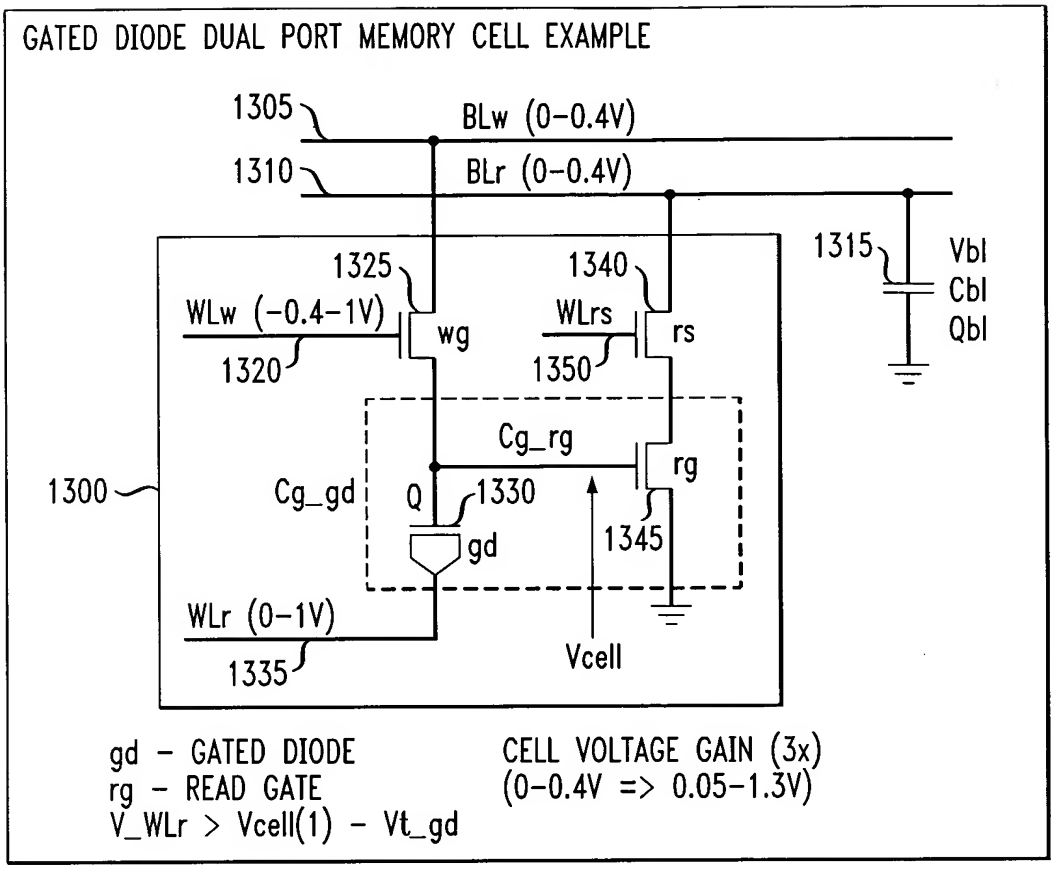

GATED DIODE DUAL PORT MEMORY CELL EXAMPLE
1305
BLw (0-0.4V)
1310
BLr (0-0.4V)
1315
Vbl
Cbl
Qbl
1325
1340
WLw (-0.4-1V)
wg
WLrs
rs
1320
1350
Cg_rg
rg
1300
Cg_gd
Q
1330
gd
1345
WLr (0-1V)
1335
Vcell
gd - GATED DIODE
rg - READ GATE
V_WLr > Vcell(1) - Vt_gd
CELL VOLTAGE GAIN (3x)
(0-0.4V => 0.05-1.3V)

FIG. 16

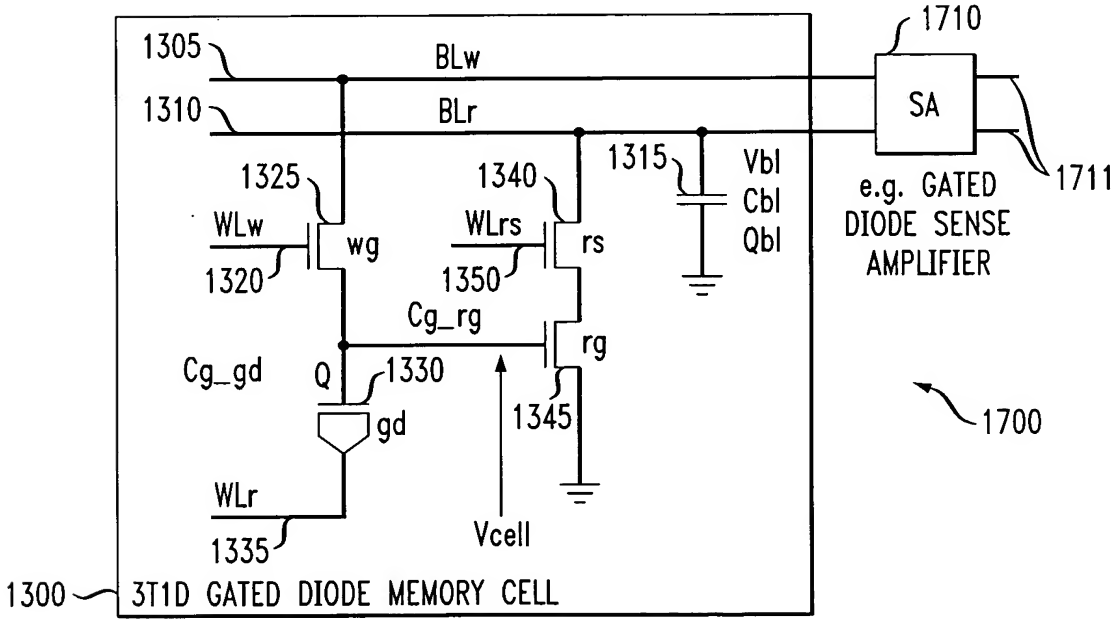

1710
1305
BLw
SA
1310
BLr
1315
Vbl
Cbl
Qbl
1325
1340
e.g. GATED
DIODE SENSE
AMPLIFIER
1711
WLw
wg
WLrs
rs
1320
1350
Cg_rg
rg
Cg_gd
Q
1330
gd
1345
1700
WLr
1335
Vcell
1300
3T1D GATED DIODE MEMORY CELL

FIG. 17

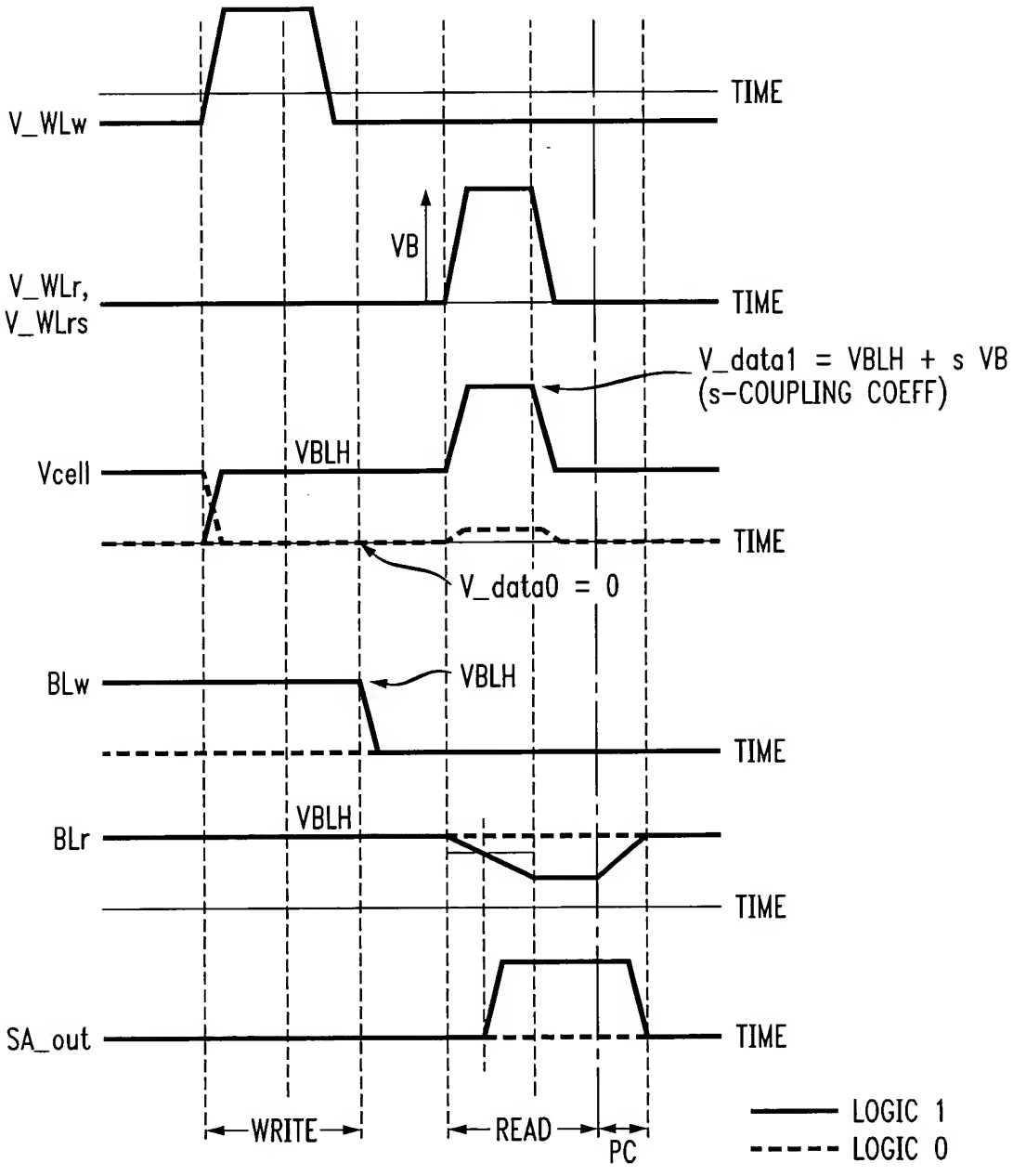

V_WLw
TIME
VB
V_WLr,
V_WLrs
TIME
V_data1 = VBLH + s VB
(s-COUPLING COEFF)
VBLH
Vcell
TIME
V_data0 = 0
BLw
VBLH
TIME
VBLH
BLr
TIME
SA_out
TIME
WRITE
READ
PC
LOGIC 1
LOGIC 0

FIG. 18

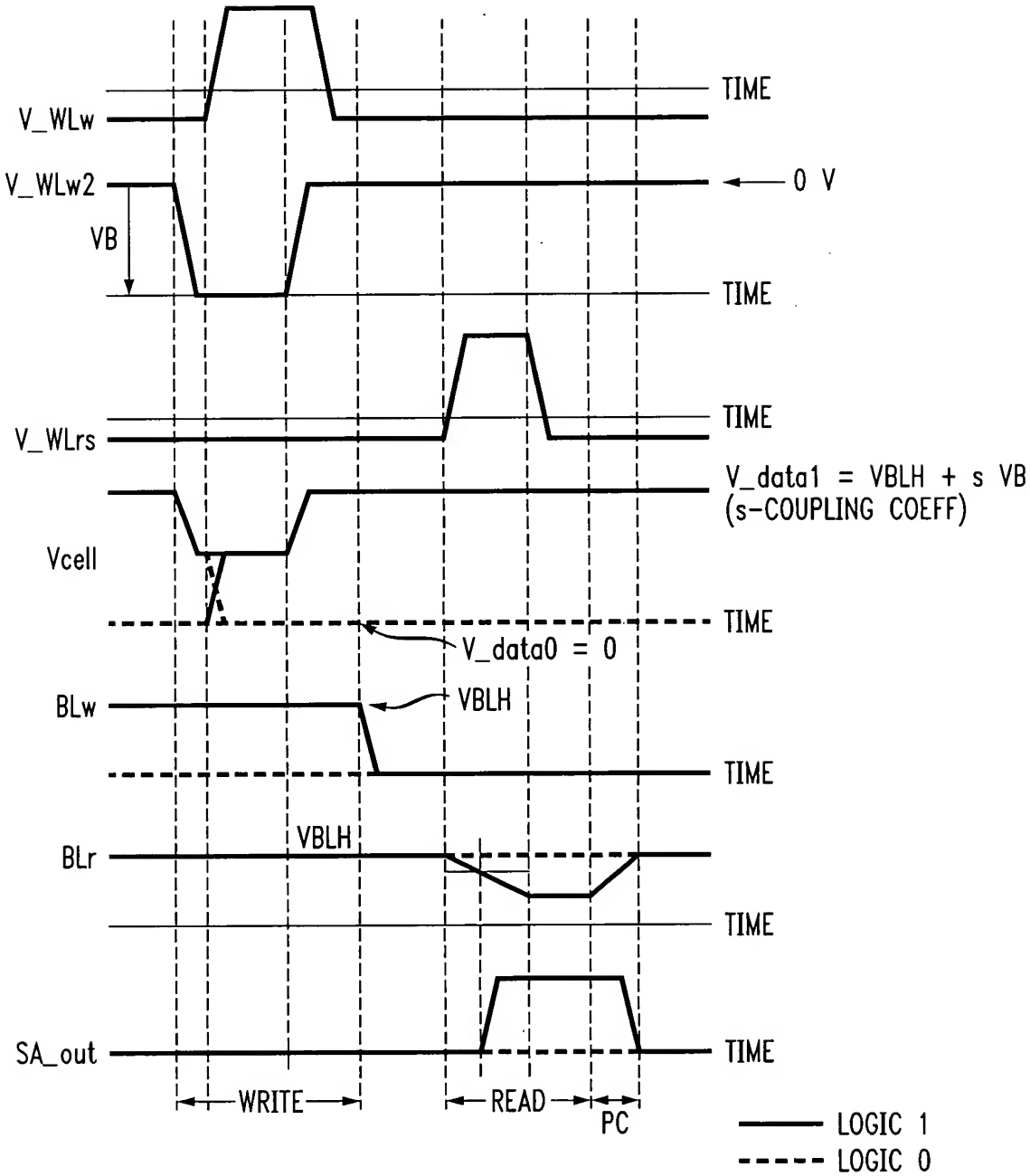

V_WLw
TIME
V_WLw2
0 V
VB
TIME
V_WLrs
TIME
V_data1 = VBLH + s VB
(s-COUPLING COEFF)
Vcell
TIME
V_data0 = 0
BLw
VBLH
TIME
BLr
VBLH
TIME
SA_out
TIME
WRITE
READ
PC
LOGIC 1
LOGIC 0

FIG. 19

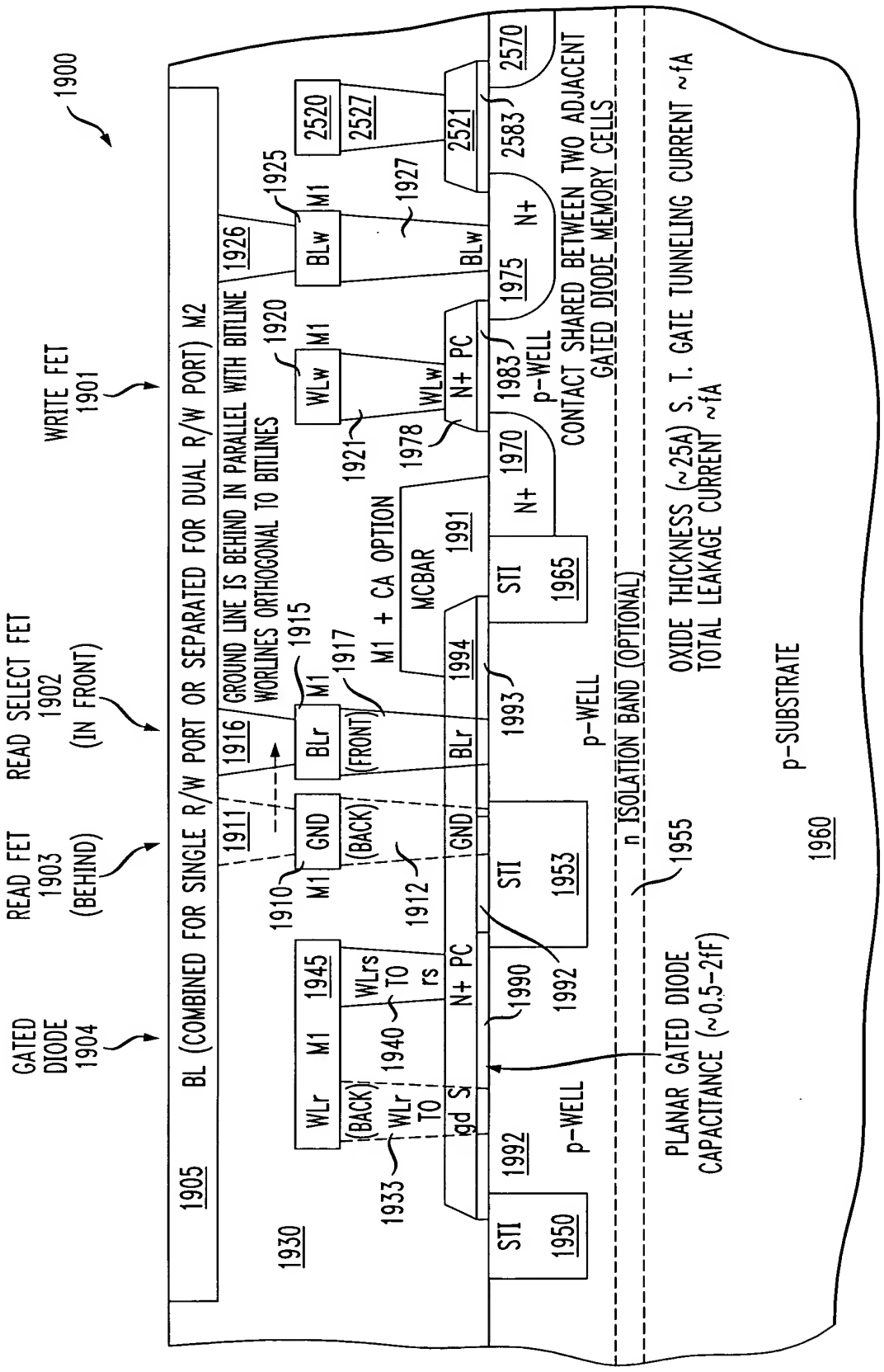

1900
GATED DIODE 1904
READ FET 1903 (BEHIND)
READ SELECT FET 1902 (IN FRONT)
WRITE FET 1901
1905 BL (COMBINED FOR SINGLE R/W PORT OR SEPARATED FOR DUAL R/W PORT) M2
1911
1916 GROUND LINE IS BEHIND IN PARALLEL WITH BITLINE
WORLINES ORTHOGONAL TO BITLINES
1926
1925
1920
1915
1917
1910
1912
1940
1933
1930
1950
1992
1990
1953
1955
1960
1994
1991
1993
1965
1970
1983
1975
1978
1921
1927
2521
2583
2570
2520
2527
WLr M1 1945
(BACK)
WLr TO
WLrs TO rs
GND
(BACK)
BLr
(FRONT)
M1 + CA OPTION
MCBAR
STI
N+ PC
gd S
p-WELL
n ISOLATION BAND (OPTIONAL)
p-SUBSTRATE
WLw M1
BLw
N+
p-WELL
CONTACT SHARED BETWEEN TWO ADJACENT GATED DIODE MEMORY CELLS
OXIDE THICKNESS (~25A) S. T. GATE TUNNELING CURRENT ~fA
TOTAL LEAKAGE CURRENT ~fA
PLANAR GATED DIODE CAPACITANCE (~0.5-2fF)

FIG. 20

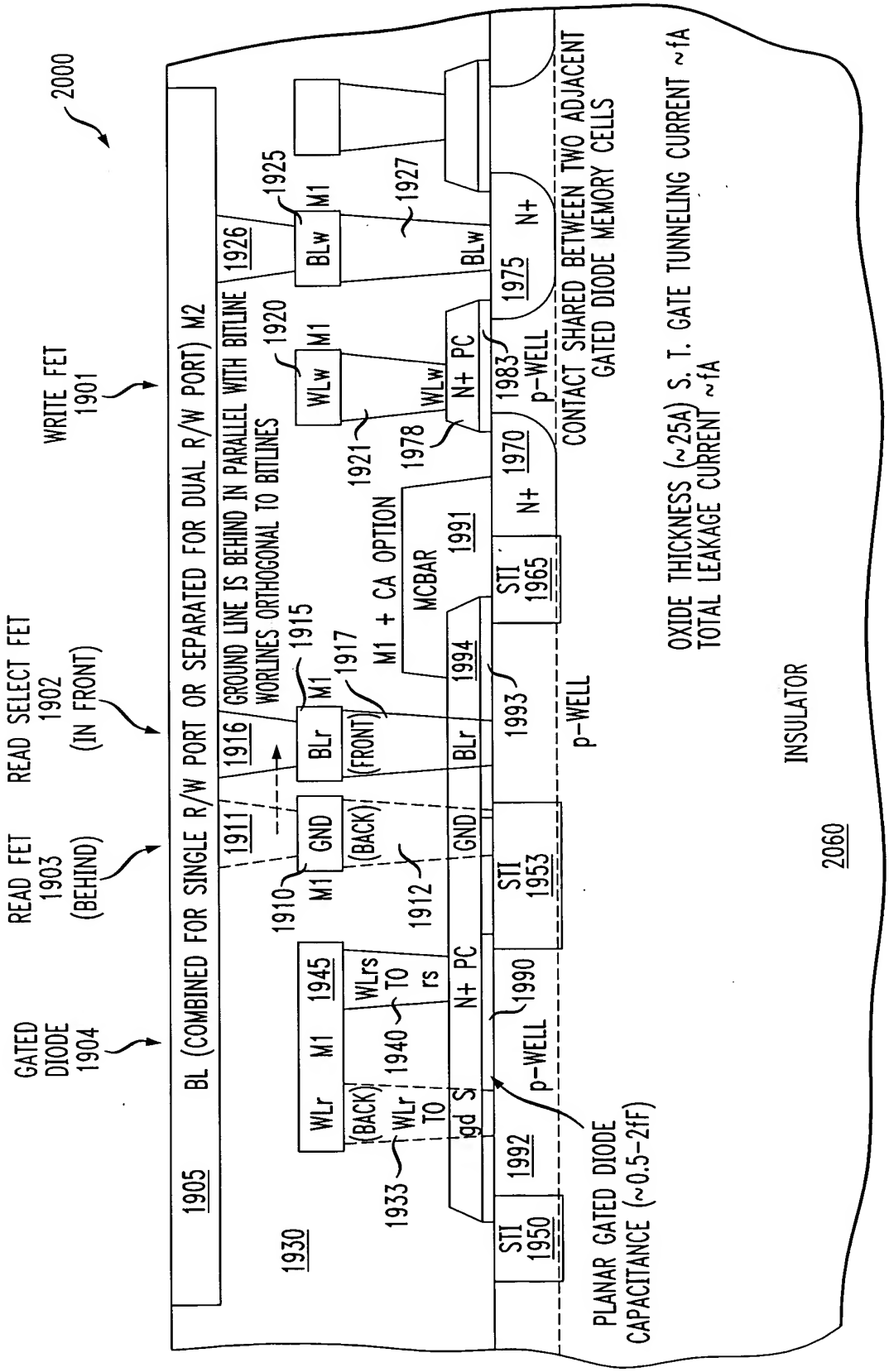

2000
GATED DIODE 1904
READ FET 1903 (BEHIND)
READ SELECT FET 1902 (IN FRONT)
WRITE FET 1901
1905 BL (COMBINED FOR SINGLE R/W PORT OR SEPARATED FOR DUAL R/W PORT) M2
1911
1916 GROUND LINE IS BEHIND IN PARALLEL WITH BITLINE
WORLINES ORTHOGONAL TO BITLINES
1926
1925
1920
1915
1917
1910
1912
1940
1933
1930
WLr M1 1945
(BACK)
WLr TO gd
WLrs TO rs
M1 GND (BACK)
BLr (FRONT)
M1 + CA OPTION
MCBAR 1991
1994
1993
1921
1978
WLw M1
WLw
N+ PC
BLw M1
BLw
1927
1983
1975 N+
p-WELL
1970 N+
STI 1965
CONTACT SHARED BETWEEN TWO ADJACENT GATED DIODE MEMORY CELLS
STI 1950
1992
p-WELL
1990
N+ PC
STI 1953
PLANAR GATED DIODE CAPACITANCE (~0.5-2fF)
p-WELL
OXIDE THICKNESS (~25A) S. T. GATE TUNNELING CURRENT ~fA
TOTAL LEAKAGE CURRENT ~fA
INSULATOR
2060

FIG. 21

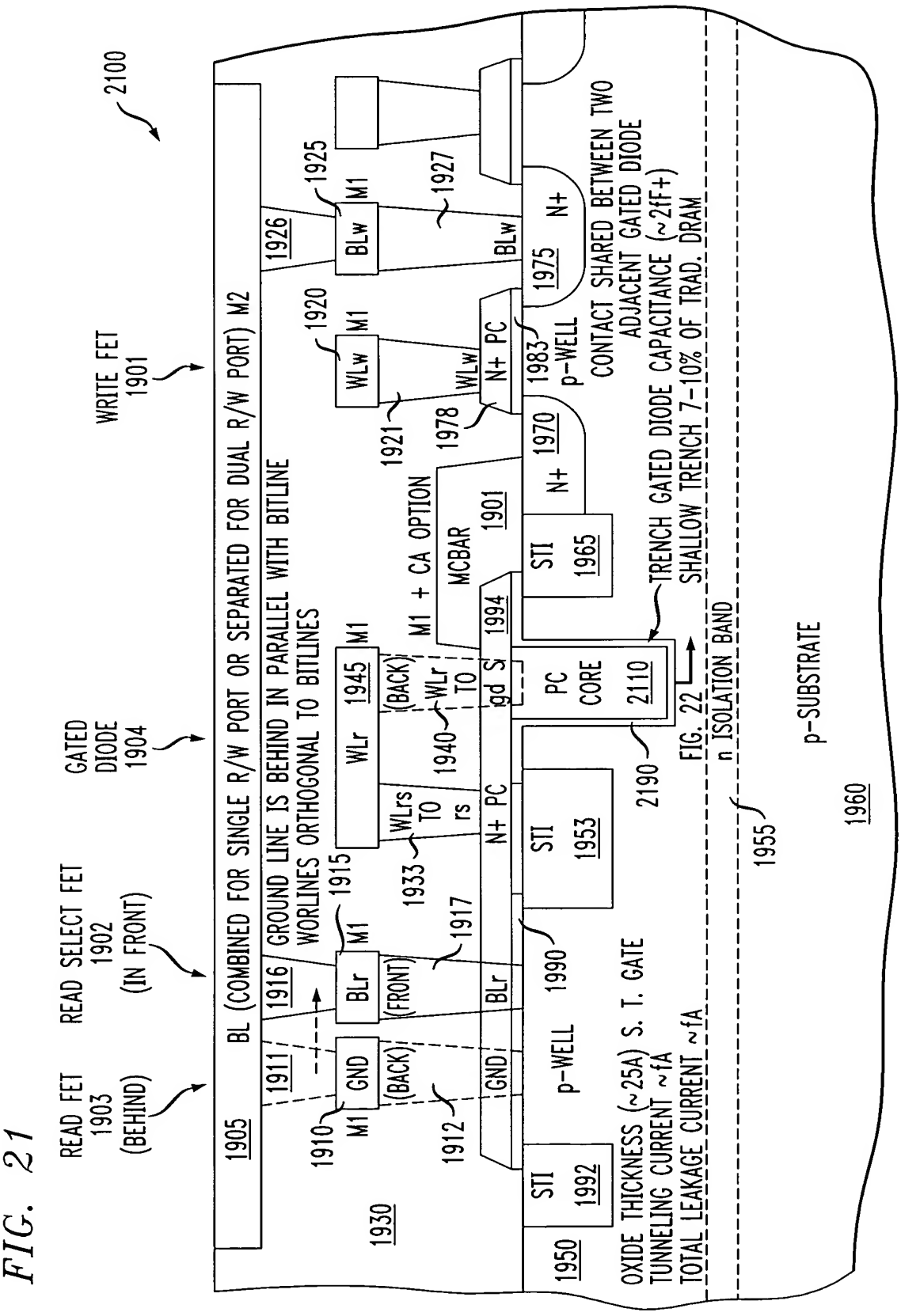

2100
READ FET 1903 (BEHIND)
READ SELECT FET 1902 (IN FRONT)
GATED DIODE 1904
WRITE FET 1901
1905 BL (COMBINED FOR SINGLE R/W PORT OR SEPARATED FOR DUAL R/W PORT) M2
1911
1916 GROUND LINE IS BEHIND IN PARALLEL WITH BITLINE
WORLINES ORTHOGONAL TO BITLINES
1926
1925
1927
1920
1921
1978
1983
1975
1970
1965
1910
1912
1915
1917
1933
1940
1945
1994
1990
1953
2110
2190
1930
1950
1992
1955
1960
GND
(BACK)
M1
BLr
(FRONT)
WLrs TO rs
WLr
TO gd S
PC CORE
STI
p-WELL
N+ PC
WLw
BLw
N+
p-WELL
MCBAR
M1 + CA OPTION
TRENCH GATED DIODE CAPACITANCE (~2fF+)
SHALLOW TRENCH 7-10% OF TRAD. DRAM
CONTACT SHARED BETWEEN TWO ADJACENT GATED DIODE
n ISOLATION BAND
p-SUBSTRATE
OXIDE THICKNESS (~25A) S. T. GATE TUNNELING CURRENT ~fA
TOTAL LEAKAGE CURRENT ~fA
FIG. 22

FIG. 22

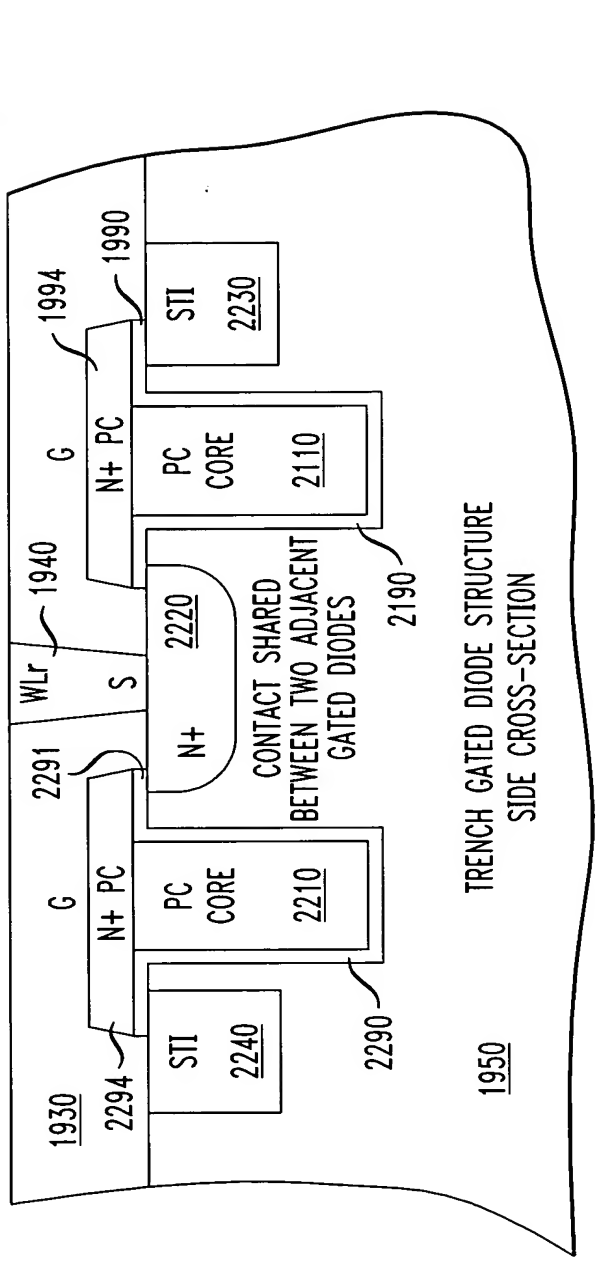

2200
1930
2294
STI
2240
G
N+ PC
2291
PC
CORE
2210
2290
WLr
1940
S
N+
2220
CONTACT SHARED
BETWEEN TWO ADJACENT
GATED DIODES
2190
1994
G
N+ PC
1990
PC
CORE
2110
STI
2230
TRENCH GATED DIODE STRUCTURE
SIDE CROSS-SECTION
1950

FIG. 23

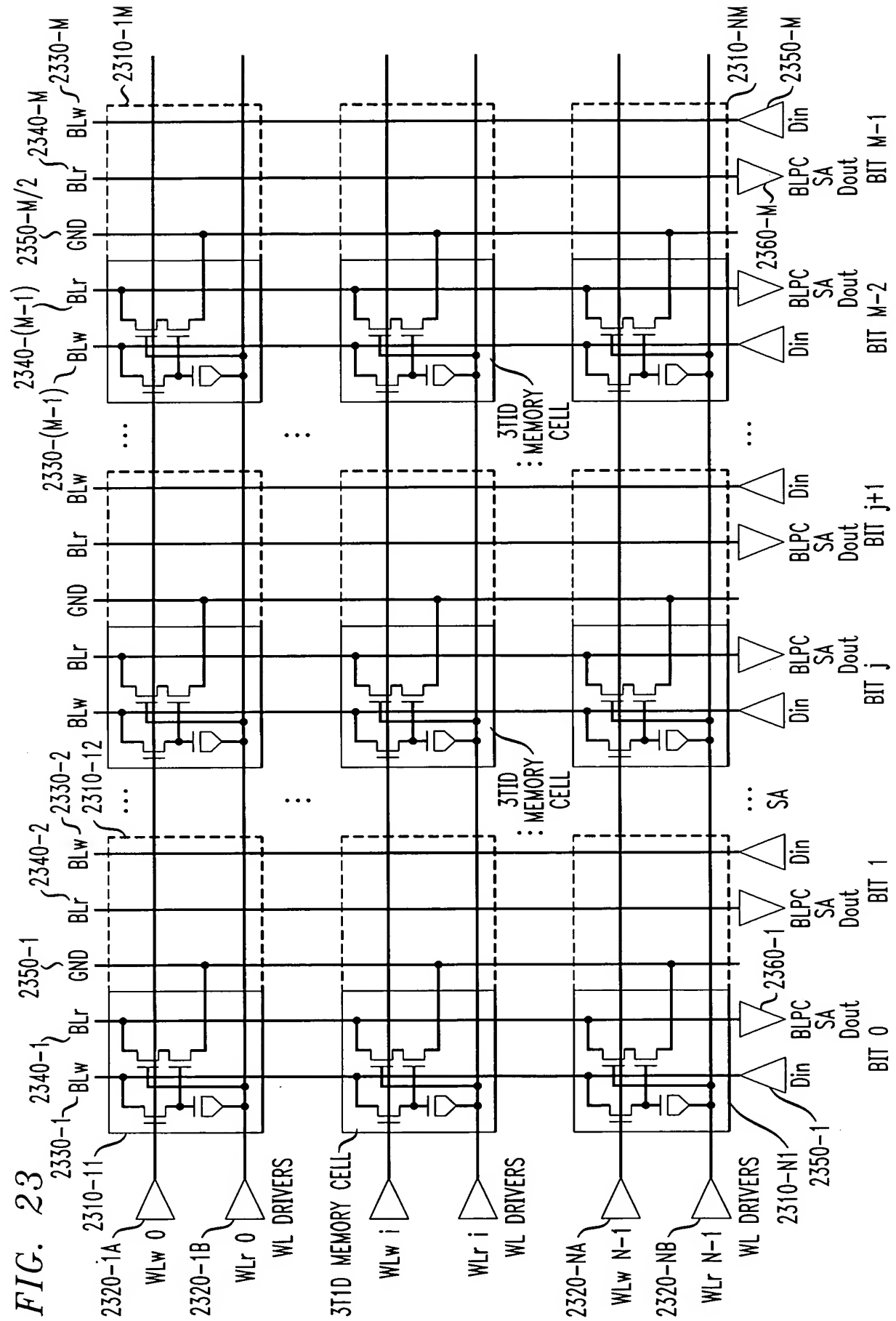

2330-1
2310-11
2340-1
BLw
BLr
2350-1
GND
BLr
2340-2
BLw
2330-2
2310-12
2330-(M-1)
2340-(M-1)
BLw
BLr
2350-M/2
GND
BLr
2340-M
BLw
2330-M
2310-1M
2310-NM
2350-M
2320-1A
WLw 0
2320-1B
WLr 0
WL DRIVERS
3T1D MEMORY CELL
WLw i
WLr i
WL DRIVERS
3TID
: MEMORY
CELL
2320-NA
WLw N-1
2320-NB
WLr N-1
WL DRIVERS
2310-N1
2350-1
Din
BLPC
SA
Dout
2360-1
2360-M
BIT 0
BIT 1
BIT j
BIT j+1
BIT M-2
BIT M-1

FIG. 24

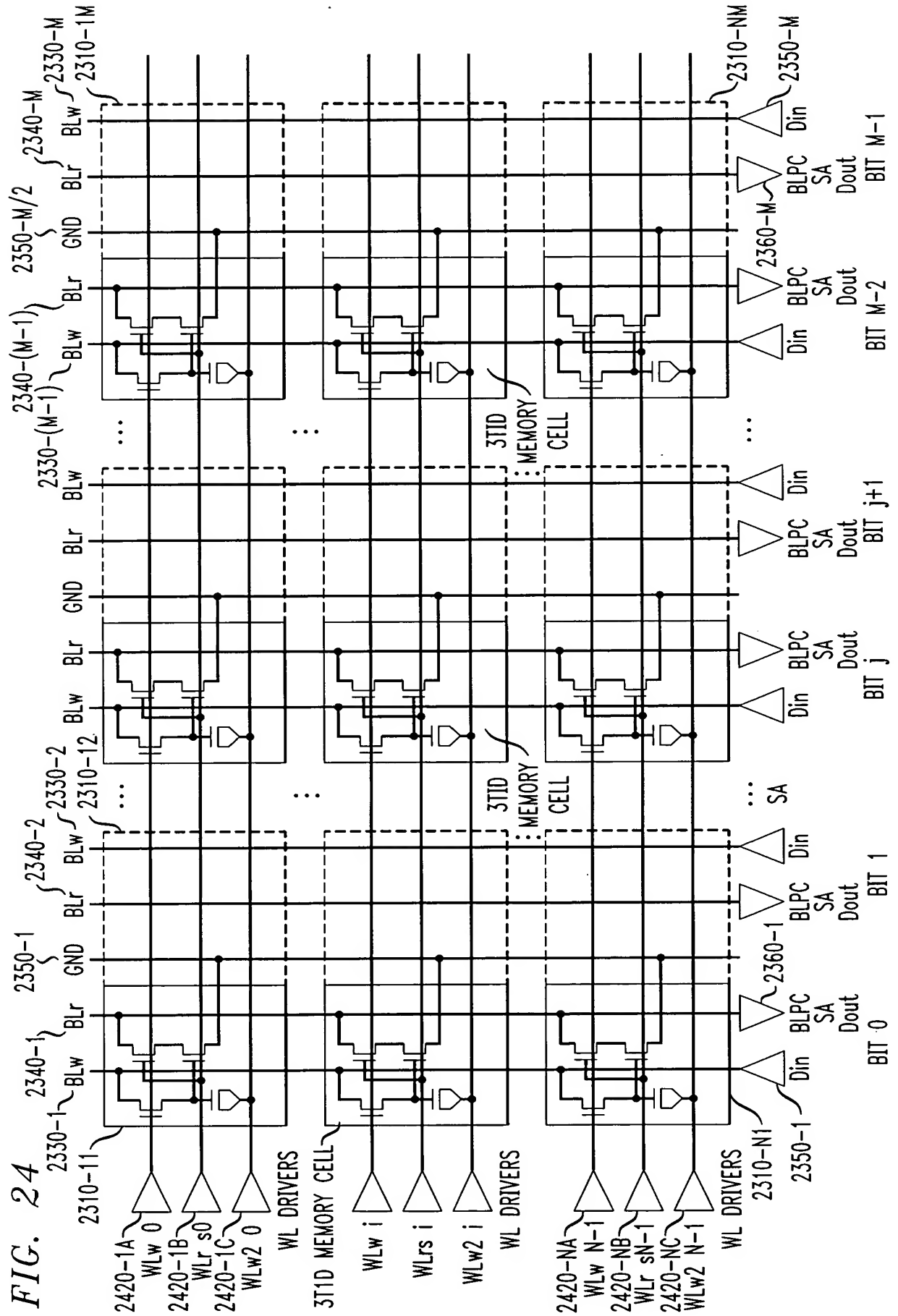

2420-1A
WLw 0
2420-1B
WLr s0
2420-1C
WLw2 0
WL DRIVERS
3T1D MEMORY CELL
WLw i
WLrs i
WLw2 i
WL DRIVERS
2420-NA
WLw N-1
2420-NB
WLr sN-1
2420-NC
WLw2 N-1
WL DRIVERS
2310-11
2330-1
2340-1
2350-1
2310-12
2330-2
2340-2
2350-1
2310-N1
2350-1
2330-(M-1)
2340-(M-1)
2350-M/2
2310-1M
2330-M
2340-M
2310-NM
2350-M
BLw
BLr
GND
Din
BLPC
SA
Dout
2360-1
2360-M
3TID
MEMORY
CELL
BIT 0
BIT 1
BIT j
BIT j+1
BIT M-2
BIT M-1

FIG. 25

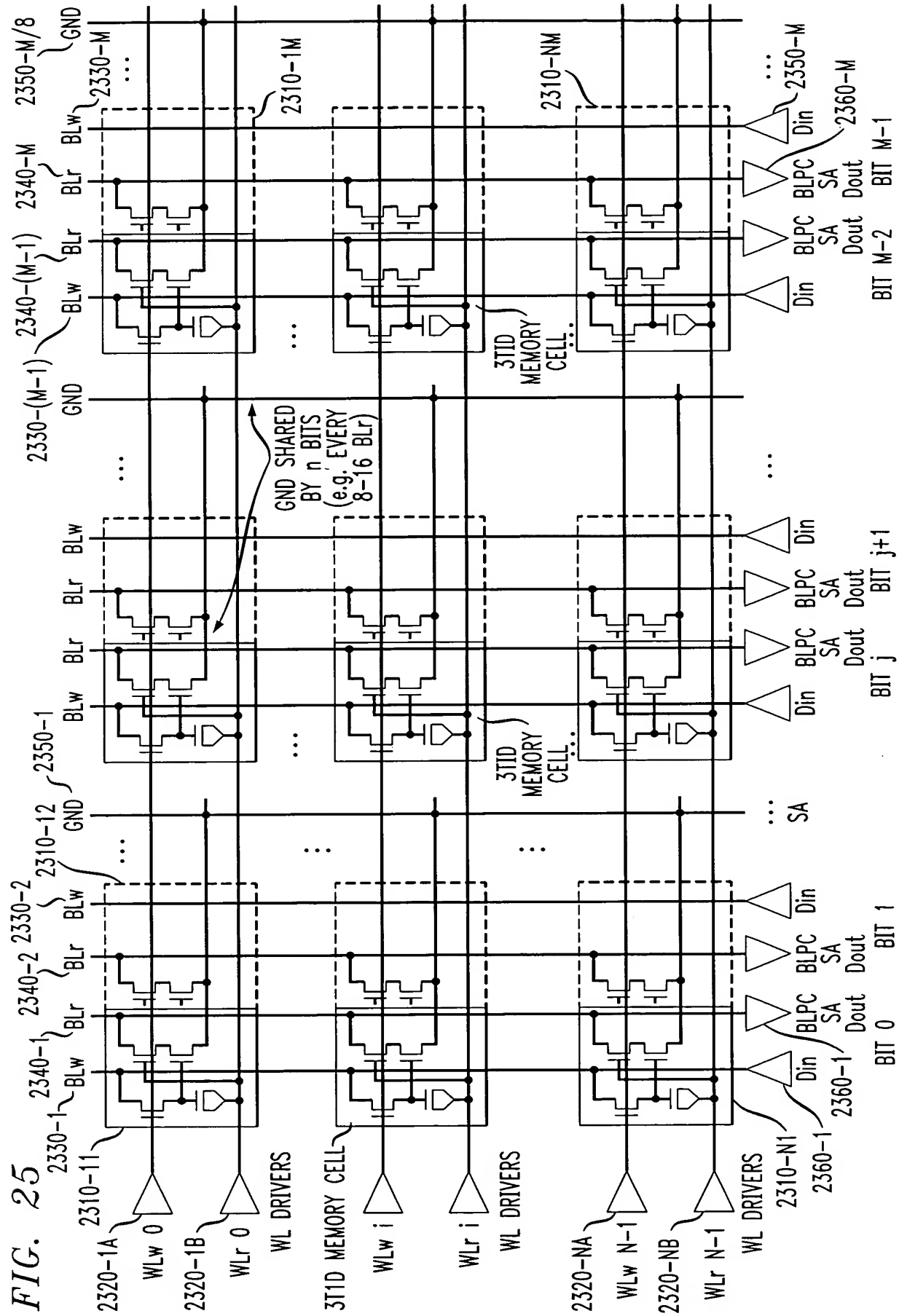
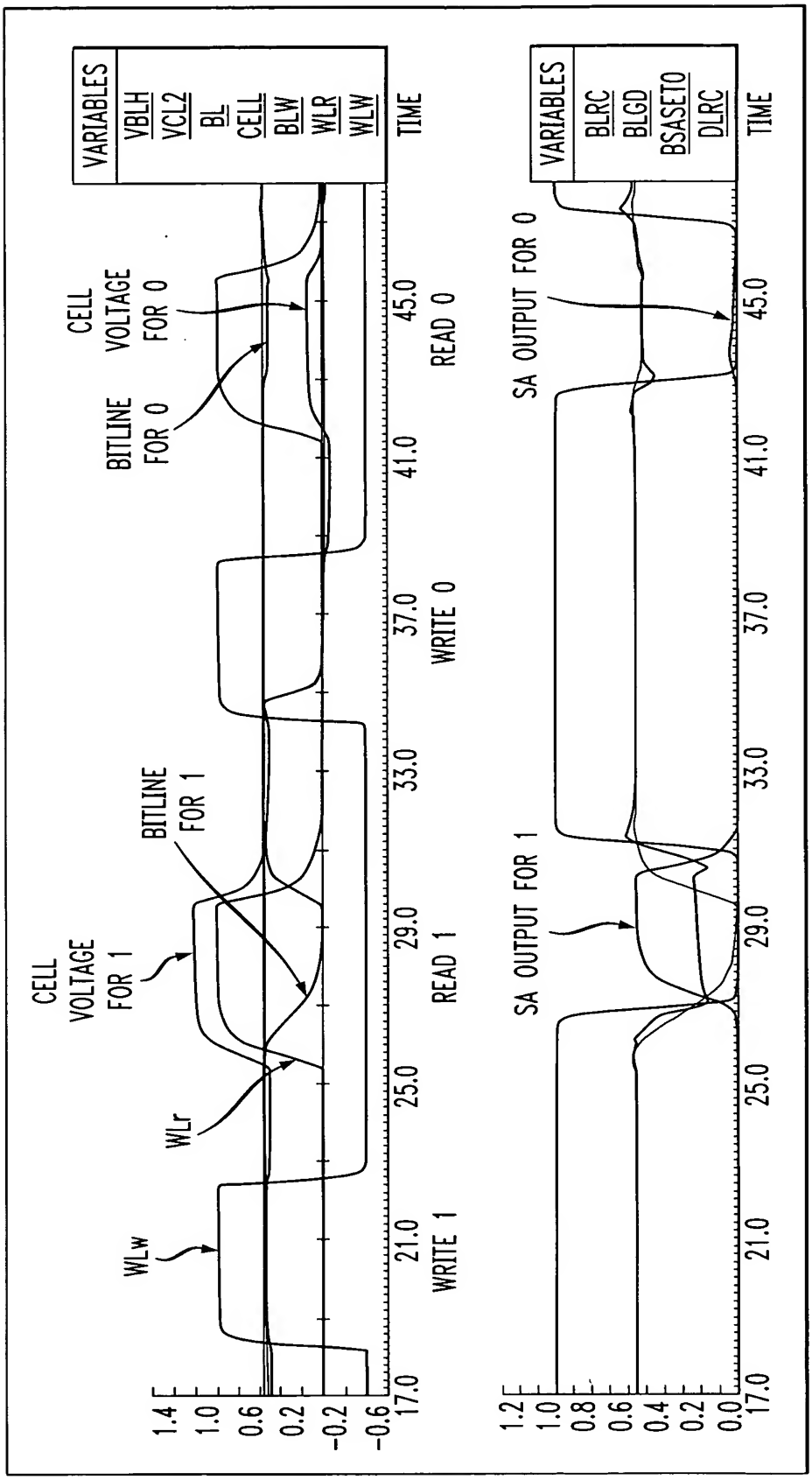

2330-1
2340-1
BLw
BLr
2310-11
2310-12
GND
2330-2
2340-2
2330-(M-1)
2340-(M-1)
2330-M
2340-M
2350-M/8
2310-1M
2310-NM
2350-1
2350-M
2360-1
2360-M
Din
BLPC
SA
Dout
BIT 0
BIT 1
BIT j
BIT j+1
BIT M-2
BIT M-1
3TID MEMORY CELL
GND SHARED BY n BITS (e.g. EVERY 8-16 BLr)
2320-1A
WLw 0
2320-1B
WLr 0
WL DRIVERS
3T1D MEMORY CELL
WLw i
WLr i
2320-NA
WLw N-1
2320-NB
WLr N-1
2310-N1

FIG. 26


VARIABLES
VBLH
VCL2
BL
CELL
BLW
WLR
WLW
TIME
CELL VOLTAGE FOR 0
BITLINE FOR 0
BITLINE FOR 1
CELL VOLTAGE FOR 1
WLr
WLw
WRITE 1
READ 1
WRITE 0
READ 0
1.4
1.0
0.6
0.2
-0.2
-0.6
17.0
21.0
25.0
29.0
33.0
37.0
41.0
45.0
VARIABLES
BLRC
BLGD
BSASETO
DLRC
TIME
SA OUTPUT FOR 0
SA OUTPUT FOR 1
1.2
1.0
0.8
0.6
0.4
0.2
0.0
17.0
21.0
25.0
29.0
33.0
37.0
41.0
45.0